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Docket No.: 64965-057 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of :

John CHIANG, et al. :

Serial No.: 09/304,964 : Group Art Unit: 2664

Filed: May 05, 1999 : Examiner: K.B. Yao

For: DYNAMIC TIME SLOT ALLOCATION IN INTERNAL RULES CHECKER SCHEDULER

TRANSMITTAL OF APPEAL BRIEF

Commissioner for Patents
Washington, DC 20231

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed July 31, 2002. Please charge the Appeal Brief fee of $320.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPEAL BRIEF

Commissioner for Patents
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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed July 31, 2002.

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., the assignee of the entire right, title and interest in and to the above-identified U. S. Application.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to the Appellant, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 2-11, and 13-18 are pending. Claims 1 and 12 are cancelled. Claims 2-11, and 13-18

stand under final rejection, from which rejection this appeal is taken.

IV. STATUS OF AMENDMENTS

After the final Office Action, claims 1 and 12 were cancelled, claims 2, 8 and 13 were rewritten in independent form. As indicated in the Advisory Action of June 25, 2002, the Amendments will be entered for purposes of Appeal.

V. SUMMARY OF INVENTION

The present invention is directed to a multiport data communication system for switching data packets between ports and having a decision making engine responsive to the received data packets for controlling transmission of the received data packets to a selected transmit port.

In a conventional communication system, each receive port is assigned with a fixed time slot, during which frame headers received from that port are transferred to processing circuitry that determines a destination station. However, data traffic at a given port may vary, so that some of the ports may become overloaded, while the others are underloaded. Hence, when no data are supplied to the frame forwarding arrangement from a given port, the bandwidth allocated to that port is wasted, whereas processing of frame headers from the overloaded ports may be delayed because the bandwidth allocated to them is not sufficient. The present invention offers a novel frame forwarding arrangement able to dynamically allocate time slots to various ports, in order to more efficiently utilize the assigned bandwidth.

As shown in Figure 1 of the application, an exemplary system in which the present invention may be advantageously employed. is a packet switched network, such as an Ethernet (IEEE 802.3) network. The packet switched network includes integrated multiport switches (IMS) 12 that enable

communication of data packets between network stations. The network may include network stations having different configurations, for example twelve (12) 10 megabit per second (Mb/s) or 100 Mb/s network stations 14 (hereinafter 10/100 Mb/s) that send and receive data at a network data rate of 10 Mb/s or 100 Mb/s, and a 1000 Mb/s (i.e., 1 Gb/s) network node 22 that sends and receives data packets at a network speed of 1 Gb/s. The gigabit node 22 may be a server, or a gateway to a high-speed backbone network. Hence, the switches 12 selectively forward data packets received from the network nodes 14 or 22 to the appropriate destination based upon Ethernet protocol.

Each switch 12 is coupled to 10/100 physical layer (PHY) transceivers 16 configured for sending and receiving data packets to and from the corresponding switch 12 across a corresponding shared media independent interface (MII) 18. In particular, each 10/100 PHY transceiver 16 is configured for sending and receiving data packets between the switch 12 and up to four (4) network stations 14 via the shared MII 18. A magnetic transformer 19 provides AC coupling between the PHY transceiver 16 and the corresponding network medium 17. Hence, the shared MII 18 operates at a data rate sufficient to enable simultaneous transmission and reception of data packets by each of the network stations 14 to the corresponding PHY transceiver 16.

As shown in Figure 2, the switch 12 contains a decision making engine 40 that performs frame forwarding decisions, a switching subsystem 42 for transferring frame data according to the frame forwarding decisions, a buffer memory interface 44, management information base (MIB) counters 48, and MAC (media access control) protocol interfaces 20 and 24 to support the routing of data packets between the Ethernet (IEEE 802.3) ports serving the network stations 14 and 22.

The switch 12 also includes a processing interface 50 that enables an external management entity such as a host CPU 32 to control overall operations of the switch 12. In particular, the processing interface 50 decodes CPU accesses within a prescribed register access space, and reads and

writes configuration and status values to and from configuration and status registers 52.

The decision making engine 40, referred to as an internal rules checker (IRC), makes frame forwarding decisions for data packets received from one source to at least one destination station. The switching subsystem 42, configured for implementing the frame forwarding decisions of the IRC 40, includes a port vector first in first out (FIFO) buffer 56, a plurality of output queues 58, a multicopy queue 60, a multicopy cache 62, a free buffer queue 64, and a reclaim queue 66.

The IRC 40 monitors (i.e., "snoops") the data bus to determine the frame pointer value and the header information of the received packet, including source, destination, and virtual LAN (VLAN) address information. The IRC 40 uses the header information to determine which MAC ports will output the data frame stored at the location specified by the frame pointer. The decision making engine may thus determine that a given data packet should be output by either a single port, multiple ports, or all ports (i.e., broadcast). For example, each data packet includes a header having source and destination address, where the decision making engine 40 may identify the appropriate output MAC port based upon the destination address. Alternatively, the destination address may correspond to a virtual address that the appropriate decision making engine identifies as corresponding to a plurality of network stations. In addition, the frame may include a VLAN tag header that identifies the frame as information destined to one or more members of a prescribed group of stations. The IRC 40 may also determine that the received data packet should be transferred to another switch 12 via the expansion port 30. Hence, the internal rules checker 40 will decide whether a frame temporarily stored in the buffer memory 36 should be output to a single MAC port or multiple MAC ports.

The internal rules checker 40 outputs a forwarding decision to the switch subsystem 42 in the form of a forwarding descriptor. The forwarding descriptor includes a port vector identifying each MAC port that should receive the data packet, priority class identifying whether the frame is high

priority or low priority, VLAN information, Rx port number, Opcode, and frame pointer. The port vector identifies the MAC ports to receive the data packet for transmission (e.g., 10/100 MAC ports 1-12, Gigabit MAC port, and/or Expansion port). The port vector FIFO 56 decodes the forwarding descriptor including the port vector, and supplies the frame pointer to the appropriate output queues 58 that correspond to the output MAC ports to receive the data packet transmission. In other words, the port vector FIFO 56 supplies the frame pointer on a per-port basis. The output queues 58 fetch the data packet identified in the port vector from the external memory 36 via the external memory interface 44, and supply the retrieved data packet to the appropriate transmit FIFO of the identified ports.

As shown in Figure 4, the IRC 40 may contain multiple rules queue 102 having frame pointers and frame header information. A single rules queue 102 may be assigned to each receive port of the IMS 12. In particular, rules queues 1 to 12 are provided for 10/100 MAC ports 1 to 12 configured to receive data from the corresponding 10/100 Mb/s network stations 14, a rules queue 13 may be arranged to support the gigabit MAC port 24 capable of receiving data from the gigabit network node 22, and a rules queue 14 may be assigned to the expansion port 30. Each rules queue 102 holds frame headers in a synchronous random access memory (SRAM) having four 40-byte entries, and stores frame pointers in a SRAM having four 13-bit entries.

The IRC 40 monitors the data bus 68 to place in each rules queue 102 the header information and frame pointers transferred by the queuing logic 74 of the corresponding receive MAC module to the external memory 36. An IRC scheduler 104 controls the transfer of data held by each rules queue 102 from the corresponding rules queue 102 to IRC logic circuits such as ingress rules logic 106, source address (SA) lookup logic 108, destination address (DA) lookup logic 110 and egress rules logic 112 to produce a forwarding descriptor supplied to the port vector FIFO 56.

The ingress rules logic 106 detects whether a frame was received with an error and checks for preset DA and VLAN information. If an error is detected or the frame address information does not match with allocated DA addresses or VLAN data, the ingress rules logic 106 produces a forwarding descriptor with a null port vector. This forwarding descriptor is transferred directly to the port vector FIFO 56 without performing SA and DA lookup operations and egress rules operations.

The SA and DA lookup logic circuits 108 and 110 search an IRC MAC address table 114 for entries associated with the MAC source and destination addresses for the corresponding frame. If source and destination address data of a frame match with the address table entries, the egress rules logic 112 checks each transmit port in the port vector list produced by the DA lookup logic circuit 110 to remove or mask the disabled ports, the ports that do not belong to a required VLAN, and the port, from which the frame is received. As a result, the egress rules logic 112 generates a forwarding descriptor including a port vector identifying each MAC port that should receive the corresponding frame.

The IRC logic circuitry performs sequential processing of data held in rules queues 102. The data from each rules queue is transferred to the IRC logic circuitry in successive time slots. The IRC scheduler 104 provides arbitration between the rules queues 102 to allocate a time slot, during which data from a given rules queue 102 will be transferred to the IRC logic circuitry. In particular, when a rules queue 102 has data to be processed by the IRC logic circuitry, the rules queue 102 sends to the IRC scheduler 104 a request for the time slot. In response, the IRC scheduler 104 produces grant signals supplied to the rules queue 102 to enable it to transfer its data to the IRC logic circuitry a frame header from a given port will be processed by during the allocated time slot.

Figure 5 illustrates an exemplary scheduling cycle of the IRC scheduler 104 having 25 time slots for the rules queues 102. Each time slot may be equal to 5 clock cycles. One time slot may be

assigned to each rules queue representing the 10/100 MAC ports 1-12, 10 time slots may be assigned to the rules queue representing the gigabit MAC port 24, and 3 time slots may be assigned to the rules queue that supports the expansion port 30.

Each individual port has a priority in accessing the time slots assigned to that port. Hence, when a rules queue 102 for a given port requests the time slot assigned to that port, its request is granted, even if the other rules queues request time slots. However, when no data are supplied to the internal rules checker from a port assigned with a current time slot, the bandwidth allocated to that port would be wasted, whereas processing of frame headers from the overloaded ports might be delayed because the bandwidth allocated to them is not sufficient.

The IRC scheduler 104 is provided with a system for dynamically allocating time slots to the rules queues 102. Referring to Figure 6, the IRC scheduler 104 operates in a free-running mode (block 202) to allocate successive time slots to rules queues 102 representing various ports. When the IRC scheduler 104 performs arbitration for access to a current time slot, it detects whether or not the rules queue 102 assigned with the current time slot requests a time slot (block 204). If a request from this rules queue is detected, then the IRC scheduler allocates the current time slot to the rules queue 102 assigned with the current time slot (block 206).

However, if no request from the current rules queue 102 is detected, the IRC scheduler 104 skips to the rules queue 102 assigned with the next time slot (block 208), and detects whether that rules queue 102 requests a time slot. If a request from the rules queue 102 assigned with the next time slot is detected, the IRC scheduler 104 allocates the current time slot to that rules queue 102 (block 212).

If no request from the next rules queue is received, the IRC scheduler 104 skips to the rules queue 102 assigned with the following time slot (block 214). The IRC scheduler 104 detects whether a

request for a time slot from the rules queue assigned with the following time slot is received (block 216), and if so the current time slot is allocated to that rules queue (block 218).

Hence the IRC scheduler 104 successively polls the rules queue assigned with time slots following the current time slot, and allocates the current time slot to the first rules queue that requests a time slot. Then, the IRC scheduler 104 goes to allocating the next time slot, and repeats operations 204 to 218 for the next time slot. Thus, time slots assigned to rules queues representing underloaded ports are dynamically allocated to rules queues representing overloaded ports.

Independent claims 2, 8 and 13 are presented below with elements read on FIGS. 1, 2, and 4 of the drawings.

2. A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports (10/100 MAC ports 1-12, gigabit MAC port 24 and expansion port 30) for receiving data packets,

a decision making engine (40) responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port (ports 1-12, 24 or 30),

the decision making engine including:

a plurality of queuing devices (102) corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry (106, 108, 110 and 112) for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler (104) interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports,

wherein the scheduler is configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

8. A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports (10/100 MAC ports 1-12, gigabit MAC port 24 and expansion port 30) for receiving data packets,

a decision making engine (40) responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port (ports 1-12, 24 or 30),

the decision making engine including:

a plurality of queuing devices (102) corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry (106, 108, 110 and 112) for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler (104) interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports,

wherein the logic circuitry comprises ingress rules logic (106) for receiving the data block to

check whether the corresponding data packets are received with an error.

13. In a communication system having a plurality of receive ports (ports 1-12, 24 and 30), at least one transmit port (ports 1-12, 24 or 30), and a decision making engine (40) for controlling data forwarding between the receive port and the at least one transmit port, a method of data processing comprising the steps of:

placing data blocks representing received data packets in a plurality of data queues corresponding to the plurality of the receive ports,

transferring the data queues in successive time slots to logic circuitry for determining the at least one transmit port, and

dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports,

wherein a data queue representing each of the receive ports is assigned with at least one of the time slots.

VI. ISSUES

Whether claims 2-11 and 13-18 are anticipated by Wu et al. (U.S. 5,771,234) under 35 U.S.C. 102(e).

VII. GROUPING OF CLAIMS

Appellant submits that the claims of each rejected group do not stand or fall together. The claims being considered to be separately patentable for the reasons presented in the Argument section of this Brief.

VIII. THE ARGUMENT

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. 102, has acquired the accepted definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." ***In re Schaumann***, 572 F.2d 312, 197 USPQ 5 (CCPA 1978). The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the Examiner. ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***In re Thorpe,*** 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); ***In re Piasecki,*** 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984). To satisfy this burden, therefore, each and every element of the claimed invention must be shown by the Examiner to be disclosed in the Wu et al. patent.

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Appellant respectfully asserts that the record fails to meet this requirement.

In particular, **independent claim 2,** among other features, recites logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in

accordance with data traffic at the corresponding receive ports. The claim requires the scheduler to be configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

The Examiner did not point out specifically wherein Wu et al. discloses the claimed scheduler configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

The reference does not expressly disclose such a scheduler, and provides no reason to conclude that the Wu arrangement inherently discloses the scheduler configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, as claim 2 requires.

Independent claim 8, among other features, recites logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet. The claim requires the logic circuitry to comprise ingress rules logic for receiving the data block to check whether the corresponding data packets are received with an error.

The Examiner did not point out wherein Wu discloses the claimed ingress rules logic. Considering the reference, no ingress rule logic in a decision making engine for controlling transmission of the received data packets is found.

Further, **independent claim 13,** among other features recites the steps of transferring the data queues in successive time slots to logic circuitry for determining the at least one transmit port, and

dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports. The claim requires a data queue representing each of the receive ports to be assigned with at least one of the time slots.

The Examiner did not point out wherein Wu discloses that a data queue representing each of the receive ports is assigned with at least one of the time slots. Instead, Wu teaches that each source is assigned with a priority state depending on various conditions. The highest priority state assigned to any source is identified. Cells of each source with the identified highest priority is assigned to a time slot (see Abstract, lines 14-25). Accordingly, only sources with the highest priority are assigned with a time slot. Hence, one skilled in the art would understand that some of the sources of Wu may be assigned with no time slots. Therefore, the reference does not disclose that a data queue representing each of the receive ports is assigned with at least one of the time slots, as claim 13 requires.

Moreover, the Examiner did not point out wherein Wu et al. discloses the subject matter of dependent **claims 3-7, 9-11 and 14-18**.

However, it is submitted that the reference does not disclose that:

- each of the plurality of the queuing devices is assigned with at least one of the time slots in each scheduling cycle (claim 3);

- the scheduler is configured to allocate a first time slot assigned to a first queuing device to a second queuing device if no request for a time slot is received from the first queuing device (claim 4);

- the second queuing device is assigned with a second time slot following the first time slot (claim 5);

- the scheduler is configured to allocate the first time slot to a third queuing device if no request for a time slot is received from the second queuing device (claim 6);

- the third queuing device is assigned with a third time slot following the second time slot

(claim 7);

- the logic circuitry further comprises source address lookup logic for comparing a source address of the data packets with a preset source address (claim 9);

- the logic circuitry further comprises destination address lookup logic for comparing a destination address of the data packets with a preset destination address (claim 10);

- the logic circuitry further comprises egress rules logic for producing a port vector identifying the at least one selected transmit port (claim 11);

- a first time slot assigned to a first data queue is allocated to the first data queue if the first data queue contains data to be processed (claim 14);

- the first time slot is allocated to a second data queue if the first data queue does not contain data to be processed (claim 15);

- the second data queue is assigned with a second time slot following the first time slot (claim 16);

- the first time slot is allocated to a third data queue if the first and second data queues do not contain data to be processed (claim 17); and

- the third data queue is assigned with a third time slot following the second time slot claim 18).

Accordingly, the Examiner has failed to show that each and every element of the claimed invention is disclosed in the Wu et al. patent, and failed to provide the extrinsic evidence that makes clear that the missing descriptive matter is necessarily present in the thing described in the reference.

IX. CONCLUSION

For the reasons advanced above, Appellant respectfully contends that the rejection of claims 2-11 and 13-18 as being anticipated under 35 U.S.C. § 102 is improper as the Examiner has not met the burden of establishing a *prima facie* case of anticipation.

Respectfully submitted,

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APPENDIX

2. A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports for receiving data packets,

a decision making engine responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port,

the decision making engine including:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports,

wherein the scheduler is configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

3. The system of claim 2, wherein each of the plurality of the queuing devices is assigned with at least one of the time slots in each scheduling cycle.

4. The system of claim 3, wherein the scheduler is configured to allocate a first time slot assigned to a first queuing device to a second queuing device if no request for a time slot is received from the first queuing device.

5. The system of claim 4, wherein the second queuing device is assigned with a second time slot following the first time slot.

6. The system of claim 5, wherein the scheduler is configured to allocate the first time slot to a third queuing device if no request for a time slot is received from the second queuing device.

7. The system of claim 6, wherein the third queuing device is assigned with a third time slot following the second time slot.

8. A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports for receiving data packets,

a decision making engine responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port,

the decision making engine including:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports,

wherein the logic circuitry comprises ingress rules logic for receiving the data block to check whether the corresponding data packets are received with an error.

9. The system of claim 8, wherein the logic circuitry further comprises source address lookup logic for comparing a source address of the data packets with a preset source address.

10. The system of claim 9, wherein the logic circuitry further comprises destination address lookup logic for comparing a destination address of the data packets with a preset destination address.

11. The system of claim 10, wherein the logic circuitry further comprises egress rules logic for producing a port vector identifying the at least one selected transmit port.

13. In a communication system having a plurality of receive ports, at least one transmit port, and a decision making engine for controlling data forwarding between the receive port and the at least one transmit port, a method of data processing comprising the steps of:

placing data blocks representing received data packets in a plurality of data queues corresponding to the plurality of the receive ports,

transferring the data queues in successive time slots to logic circuitry for determining the at least one transmit port, and

dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports,

wherein a data queue representing each of the receive ports is assigned with at least one of the time slots.

14. The method of claim 13, wherein a first time slot assigned to a first data queue is allocated to the first data queue if the first data queue contains data to be processed.

15. The method of claim 14, wherein the first time slot is allocated to a second data queue if the first data queue does not contain data to be processed.

16. The method of claim 15, wherein the second data queue is assigned with a second time slot following the first time slot.

17. The method of claim 16, wherein the first time slot is allocated to a third data queue if the first and second data queues do not contain data to be processed.

18. The method of claim 17, wherein the third data queue is assigned with a third time slot following the second time slot.